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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,575	09/25/2004	Yu-Fang Tsai	10792-US-PA	5574

31561 7590 02/23/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,575	TSAI ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 2, line 4 the phrase "connected one" appears to be missing a preposition. Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6-8, 10-15 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn, US patent No. (5,962,810) in view of Mostafazadeh et al. US patent No. (5,783,870).

Regarding claims 1, Glenn teaches a chip packaging unit comprising a substrate (11), having a top surface (12) and a corresponding bottom surface (13), a plurality of upper contacts (17) disposed on the top surface (12), and a plurality of lower contacts (31) disposed on the bottom surface (13), wherein the upper contacts (17) are electrically connected to the lower contacts respectively (31); a chip (14) disposed on the top surface of the substrate and having a plurality of inner contacts (19) and a

plurality of outer contacts (col. 3, lines 20-22 says non-optical circuitry), wherein the inner contacts are electrically connected to the outer contacts respectively (electrical connection between the outer contacts and the inner contacts established via 14); a plurality of wires (18), respectively connected to the upper contacts (17) and the inner contacts (19); a molding compound (20) covering the wires, the chip and the upper contacts of the substrate, wherein the molding compound has an opening for exposing the outer contacts (refer to fig. 1); and a plurality of solder balls (33), respectively connected to the lower contacts.

Glenn does teach a chip-packaging stack structure, comprising: a plurality of chip-packaging units, suitable for stacking one over another, lower contacts corresponding to the outer contacts of other chip-packaging units for electrically connecting the chip-packaging units.

Mostafazadeh teaches chip package of stacked ball grid array (fig. 4A) with a plurality of chip-packaging units (32), suitable for stacking one over another (refer to fig. 4A), where lower contacts (end point of 54) corresponding to the outer contacts (40) of other chip-packaging units for electrically connecting the chip-packaging units. Furthermore Mostafazadeh teaches plurality of outer contacts (pads 40 arranged at the center).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to stack the structure taught by Glenn as taught by Mostafazadeh in order to use less printed circuit board area. The modified structure of Glenn and

Mostafazadeh would have lower contacts corresponding to the outer contacts of other chip-packaging units for electrically connecting the chip-packaging units.

Regarding claim 2, Glenn teaches substantially the entire claimed structure of claim 1 above including the outer contacts (col. 3, lines 20-22 says non-optical circuitry and also the modified structure would have the pads 40) in the central area are disposed in central area on a surface of the chip, and the inner contacts (19) are disposed in a periphery area on a surface of the chip.

Regarding claim 3, Glenn teaches substantially the entire claimed structure of claim 1 above including the outer contacts (40, refer to fig. 3A of Mostafazadeh) are disposed in a surface array distribution.

Regarding claim 4, Glenn teaches substantially the entire claimed structure of claim 1 above including the outer contacts (40) are corresponding to the lower contacts (54), and the lower contacts are disposed in a surface array distribution in a central area of a surface of the bottom surface (refer to fig. 4A, where the contacts 54 are arranged as an array).

Regarding claim 6, Glenn teaches substantially the entire claimed structure of claim 1 above including the chip further comprises a plurality of bonding pads (19 of Glenn), a portion of which constitute the inner contacts (19), and the other portion of which constitute the outer contacts (40 of Mostafazadeh).

Regarding claim 7, Glenn teaches substantially the entire claimed structure of claim 1 above including the chip-packaging units is disposed in a distribution of a ball grid array (refer to fig. 4A of Mostafazadeh and fig. 1 of Glenn).

Regarding claim 8, Glenn teaches substantially the entire claimed structure of claim 1 above the substrate is made of ceramic (col. 2, lines 62-65, Glenn).

Regarding claim 10, Glenn a first chip-packaging unit, having a substrate (11) and a first chip (14), wherein the substrate has a top surface (12) and a corresponding bottom surface (13), a plurality of upper contacts (17) disposed on the top surface (12), a plurality of lower contacts (31) disposed on the bottom surface (13) and electrically connected (via 15) to the upper contacts respectively, and wherein the first chip (14) is disposed on the top surface (12) and electrically connected to the upper contacts (17).

Glenn does not teach a second chip-packaging unit having a carrier and a second chip disposed on the carrier, wherein the second chip has a plurality of inner contacts and a plurality of outer contacts, and the inner contacts are electrically connected to the carrier; and a plurality of solder balls, respectively connected to the lower contacts and the outer contacts such that the first chip-packaging unit and the second chip packaging unit are stacked and electrically connected.

Mostafazadeh teaches chip-packaging unit (refer to fig. 4A of Mostafazadeh), having a carrier (60) and a plurality of chips (46) disposed on the carrier, wherein the second chip has a plurality of inner contacts and a plurality of outer contacts (array of conductive pads 40), and the inner contacts are electrically connected to the carrier (contacts made through solder balls 42); a plurality of solder balls (42), respectively connected to the lower contacts and the outer contacts such that the first chip-packaging unit and the second chip packaging unit are stacked and electrically connected (refer to fig. 4A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to stack the structure taught by Glenn as taught by Mostafazadeh in order to use less printed circuit board area. The modified structure of Glenn and Mostafazadeh would the lower contacts and the outer contacts such that the first chip-packaging unit and the second chip-packaging unit are stacked and electrically connected.

Regarding claims 11-13, Glenn teaches substantially the entire claimed structure of claims 2, 3 and 10 above including the outer contacts (col. 3, lines 20-22 says non-optical circuitry and also the modified structure would have the pads 40) are disposed in a central area on a surface of the second chip, and the inner contacts (outer portion of 40) are disposed in a periphery area on a surface of the second chip.

Regarding claim 14, Glenn teaches (fig. 1) substantially the entire claimed structure of claim 1 above including a chip-packaging unit comprising: a substrate (11), having a top surface (12) and a corresponding bottom surface (13), a plurality of upper contacts (17) disposed on the top surface, and a plurality of lower contacts (31) disposed on the bottom surface, wherein the upper contacts are electrically connected to the lower contacts respectively (via 15); a chip (14), disposed on the top surface of the substrate and having a plurality of inner contacts (19) and a plurality of outer contacts (col. 3, lines 20-22 says non-optical circuitry and pads 40 arranged at the center); a plurality of wires (18), respectively connected to the upper contacts (17) and the inner contacts (19); and a molding compound (20), covering the wires (18), the chip

(14) and the upper contacts (17) of the substrate, and having an opening for exposing the outer contacts.

Regarding claim 15, Glenn teaches substantially the entire claimed structure of claim 14 above including plurality of solder balls (33) disposed respectively on the lower contacts (31).

Regarding claim 17, Glenn teaches substantially the entire claimed structure of claim 14 above including the chip further comprises a plurality of bonding pads (19 of Glenn), a portion of which constitute the inner contacts (19), and the other portion of which constitute the outer contacts (40 of Mostafazadeh).

Regarding claim 18, Glenn teaches substantially the entire claimed structure of claim 14 above including the substrate is made of ceramic (col. 2, lines 62-65, Glenn).

4. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn, Mostafazadeh and in view of Hsuan et al. US patent No. (6,166,444).

Regarding claims 5 and 16, Glenn teaches substantially the entire claimed structure of claims 1 and 14 above except explicitly stating the chip further comprises a plurality of bonding pads and a redistribution layer disposed on a surface of the chip, and the bonding pads are respectively connected through the redistribution layer to the inner contacts and the outer contacts.

Hsuan teaches the use of redistribution layer (46) in order to make contact to bonding pad structure (42) in the structure of forming a packaging device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the redistribution layer taught by Hsuan in the structure of Glenn in order to form contact between the chip and the bonding pads.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn, Mostafazadeh and in view of Shibata et al. US patent No. (6,586,832).

Glenn teaches substantially the entire claimed structure of claim 1 above except explicitly stating a heat dissipating plate, disposed on the top layer of the chip-packaging units and in the opening of the molding compound of the top layer.

Shibata teaches (fig. 1) the use of heat dissipating plate (6) attached to the top surface of the chip (2) in order to dissipate heat from the semiconductor chip (2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the heat dissipating plate taught by Shibata in the structure of Glenn in order to dissipate heat from the chip.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References E and F are cited as being related to packaging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
February 16, 2005

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